Sub 09

Claim 30. The method as claimed in claim 24, further comprising forming a dielectric layer by:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

By Sub 08

Claim 31. (New) A method for etching a semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

depositing a layer of germanium over the dielectric layer;

patterning the layer of germanium to form a germanium hard mask;

patterning the dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the dielectric layer; and

selectively etching the semiconductor substrate through the opening in the dielectric layer.

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Claim 32. (New) The method as claimed in claim 31, further comprising the step of stripping away the germanium hard mask after patterning the dielectric layer.

REMARKS

Claims 1-30 are currently pending in the application. Applicants have amended claims 1, 9 and 15, and have added new claims 22-30. Applicants request reconsideration of the application in light of the following remarks.

Rejections under 35 U.S.C. § 112

Claim 21 stands rejected by the Examiner under 35 U.S.C. 112. Claim 21 recites the step of "removing the layer of photoresist prior to the step of selectively etching the dielectric layer through the germanium hard mask." As stated by the Examiner, Applicants' specification states "After etching layer 22 of metallic germanium, photoresist layer 24 is stripped away using techniques known in the art." The Examiner acknowledges that the techniques of stripping away photoresist layers are well known in the art, but asserts that it is generally not well known in the art how to strip photoresist material over metallic germanium without stripping the metallic germanium. The Examiner cites the disclosure of Jeungling to explain the "techniques known in the art."

It is well known in the art that metallic germanium is generally a stable material until it is oxidized, and that photoresist is commonly removed from underlying stable layers using well known photoresist stripping processes. Common photoresist stripping processes are also sufficient to remove the photoresist from the underlying metallic germanium layer without removing the metallic germanium. This is shown and described in the reference cited by the Examiner to Jeungling. As shown in FIG. 3 of Jeungling and described at col. 3, lines 60-65, the photoresist stripping process used by Jeungling removes the photoresist layer from off of the underlying germanium layer 16, referenced at times t1, t2, t3 and t4, without affecting the underlying germanium layer 16. As explained in Applicants' previous response, because the germanium layer used in Jeungling is considered relatively useless to the process of Jeungling after the photoresist has been patterned, there is no need to preserve it by completing the photoresist strip process. Rather than completely remove the photoresist by completing the photoresist strip process Jeungling applies a piranha clean process to remove the germanium layer once a sufficient amount of germanium is revealed to allow the germanium to be dissolved by the piranha clean. *See* Jeungling, col. 3, line 66 to col. 4, line 4. Because the remaining photoresist residue is removed as a result of the germanium layer being gone, there is no need to complete the photoresist stripping process.

Jeungling's choice to use pirhana clean to remove the germanium layer before the photoresist residue is removed does not imply that it is unknown in the art to remove photoresist from germanium without simultaneously removing the germanium Applicants' disclosure sufficiently identifies that conventional photoresist stripping processes are sufficient to remove photoresist from an underlying metallic germanium layer. This disclosure is supported by the disclosure of Jeungling (col. 3, lines 60-65). Cho also mentions removal of photoresist by an ashing/strip process. *See* Cho, col. 4, lines 22-24. Applicants respectfully request that the rejection of claim 21 under 35 U.S.C. § 112 be withdrawn.

Rejections under 35 U.S.C. § 103

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based upon the Applicants' disclosure. A failure to meet any one of these criteria is a failure to establish a *prima facie* case of obviousness. MPEP §2143.

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho et al. (U.S. Patent No. 6,074,930, hereinafter "Cho") in view of Juengling (U.S. Patent No. 5,750,442, hereinafter "Juengling"). Applicants respectfully traverse this rejection and request reconsideration of the amended claims.

Both claims 1 and 9, as amended, recite a "germanium hard mask as a top most layer over the dielectric" and "etching the dielectric . . . through the germanium hard mask with the germanium hard mask as a top most layer . . . ." As explained in Applicants' previous response, a combination of the teachings of Jeungling and Cho would not result in the use of the germanium layer of Jeungling as a hard mask. Rather, if the germanium layer of Jeungling were incorporated into the process of Cho, based upon the combined teachings of Jeungling and Cho, it would only be used as part of the photoresist process to pattern an underlying hard mask, and would then be removed with the photoresist before subsequent etching of a layer beneath the resulting hard mask.

Cho offers no teachings or suggestions on the use of a germanium layer, but does mention the use of a hard mask patterned by a photolithographic process using photoresist. *See* Cho, col. 3, line 61 to col. 4, line 21. Jeungling does not teach the use of a hard mask, but teaches the use of a germanium layer in combination with a photolithographic process used to etch a dielectric. *See* Jeungling, col. 3, line 51 to col. 4, line 9. According to the teachings of Jeungling, the germanium layer is removed after the photoresist layer is removed and prior to further processing of the semiconductor substrate. If used in combination with the disclosure of Cho, the germanium layer, therefore, would also be removed after the photoresist layer is removed and before further processing of the substrate. Contrarily, Applicants claims 1 and 9 recite use of the germanium layer as a top most layer over the dielectric while etching the dielectric. Thus, the germanium layer is not removed after a photoresist layer is removed and before further processing of the substrate, contrarily the dielectric layer is etched while the germanium layer is still in place, using the germanium as a germanium hard mask. The claimed methods of independent claims 1 and 9 are not taught or suggested by the combined teachings of Jeungling and Cho, and are therefore allowable. Dependent claims 2-8 and 10-14 are allowable, among other reasons, for depending from allowable claims 1 and 9.

Similar to claims 1 and 9, independent claim 15, as amended, recites "forming a germanium hard mask as a top most layer over the dielectric stack; [and] etching the dielectric stack through the germanium hard mask to form a dielectric hard mask . . . ." As explained with respect to claims 1 and 9 and in Applicants' previous response, a combination of the teachings of Jeungling and Cho would not result in the use of the germanium layer of Jeungling as a hard mask or as a germanium hard mask as a top most layer over the dielectric stack. A combination of the teachings of Jeungling and Cho would only use the germanium layer as part of the photoresist process and would remove the germanium layer prior to an opportunity to use it as a germanium hard mask in subsequent etching of the dielectric stack. The claimed method of independent claim 15 is not taught or suggested by the combined teachings of Jeungling and Cho, and is therefore allowable. Dependent claims 16-21 are allowable, among other reasons, for depending from allowable claim 15.

To be clear and not imply agreement to the Examiner's interpretation of Applicants' arguments found on page 4, paragraph 8, last sentence of the most recent Office Action, Applicants did not assert that the "germanium material of Jeungling is completely removed prior to any etching of the lower layers". Rather, Applicants accurately stated that "The germanium layer and dielectric layers are all etched according to the patterned photoresist layer using an ansiotropic etch. . . . The germanium layer and photoresist layer are then completely removed before the semiconductor substrate is processed. *See* Jeungling col. 3, line 60 to col. 4, line 17."

Applicants respectfully request that the obviousness rejections of claims 1-21 be withdrawn.

New Claims 22-32

Claims 22 and 23 are allowable for depending indirectly from allowable claims 1 and 9 respectively. Additionally, claims 22 and 23 are allowable for reciting "removing the

photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask." As explained in support of claims 1 and 9, the combined teachings of Jeungling and Cho teach to etch the dielectric layer before removing the photoresist layer. Independent claim 24 recites "patterning the dielectric layer through the germanium hard mask after removing the photoresist layer from over the germanium hard mask . . . ." As stated in support of claims 1, 9 and 15, the combined teachings of Jeungling and Cho teach to etch the dielectric layer before removing the photoresist layer. Claims 25-30 depend from claim 24.

Independent claim 31 recites "patterning the dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the dielectric layer . . . ." The process disclosed in Jeungling, which includes a germanium layer, etches both the germanium layer and the dielectric layer at the same time. Thus, its process is not selective to germanium because it removes the germanium layer. The combined teachings of Jeungling and Cho do not teach or suggest selectively etching the dielectric layer without etching a germanium hard mask. For the invention of claim 31, by patterning the dielectric layer through the germanium hard mask using a process selective to germanium, the openings in the dielectric layer may be formed in the pattern of the germanium hard mask without depleting the germanium hard mask. Thus, the invention of claim 31 is not taught or suggested by the combined teachings of Jeungling and Cho. Claim 32 depends from claim 24.

In summary, and in view of the amendments herein, none of the references cited by the Examiner nor any other known prior art, either alone or in combination, disclose the unique combination of features disclosed in applicant's claims presently on file. For this reason, allowance of all of applicant's claims is respectfully solicited.

Regarding Doctrine of Equivalents

Applicants hereby declare that any amendments herein that are not specifically made for the purpose of patentability are made for other purposes, such as clarification, and

that no such changes shall be construed as limiting the scope of the claims or the application of the Doctrine of Equivalents.

CONCLUSION

The amendments herein added 2 new independent and 9 new dependent claims. There is also a Request for Continued Examination resulting in fees due of $ 740.00 . If any additional fees, including extension of time fees or additional claims fees, are due as a result of this response, please charge IBM Corp. Deposit Account No. 09-0456. This authorization is intended to act as a constructive petition for an extension of time, should an extension of time be needed as a result of this response. The examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this case.

Respectfully submitted,

Date: November 12, 2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claim 1. (Twice Amended) A method for etching a semiconductor substrate using a germanium hard mask, the semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

depositing a layer of metallic germanium over the dielectric layer;

patterning the layer of metallic germanium to form the germanium hard mask as a top most layer over the dielectric layer;

selectively etching the dielectric layer through the germanium hard mask with the germanium hard mask as a top most layer to form an opening in the dielectric layer; and

selectively etching the semiconductor substrate through the opening in the dielectric layer.

Claim 2. (Unchanged) The method as claimed in claim 1, further comprising the step of stripping away the layer of metallic germanium after performing the step of selectively etching the dielectric layer.

Claim 3. (Unchanged) The method as claimed in claim 2, the step of stripping away the layer of metallic germanium including the steps of:

oxidizing the layer of metallic germanium to form a layer of germanium oxide therefrom; and

removing the layer of germanium oxide.

Claim 4. (Unchanged) The method as claimed in claim 3, the step of removing the layer of germanium oxide including rising the semiconductor substrate in water.

Claim 5. (Unchanged) The method as claimed in claim 2, the step of stripping away the layer of metallic germanium including stripping away the layer of metallic germanium before performing the step of selectively etching the semiconductor substrate.

Claim 6. (Unchanged) The method as claimed in claim 1, the step of depositing a layer of metallic germanium including depositing the layer of metallic germanium having a thickness between approximately 40 nm and approximately 500 nm.

Claim 7. (Unchanged) The method as claimed in claim 1, the step of patterning the layer of metallic germanium further including the steps of:

depositing a photo resist layer over the layer of metallic germanium;

exposing and developing the photo resist layer to form a photolithography image; and

etching the layer of metallic germanium through the photolithography image.

Claim 8. (Unchanged) The method as claimed in claim 1, the step of forming a dielectric layer further including the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

Claim 9. (Twice Amended) A method for fabricating a semiconductor device having a dielectric stack over a major surface thereof, comprising the steps of:

depositing a metallic germanium layer over the dielectric stack;

patterning the metallic germanium layer to form a germanium hard mask as a top most layer over the dielectric stack;

etching the dielectric stack through the germanium hard mask with the germanium hard mask as a top most layer to form a dielectric hard mask over the major surface of the semiconductor substrate;

etching the semiconductor substrate through the dielectric hard mask;

forming doped regions in the semiconductor substrate; and

forming dielectric and conductive structures over the semiconductor substrate.

Claim 10. (Unchanged) The method as claimed in claim 9, further comprising the step of stripping away the metallic germanium layer after the step of etching the dielectric stack and before the step of etching the semiconductor substrate.

Claim 11. (Unchanged) The method as claimed in claim 10, wherein the step of stripping away the metallic germanium layer includes the steps of:

oxidizing the metallic germanium layer; and

rising the semiconductor substrate in water.

Claim 12. (Unchanged) The method as claimed in claim 9, wherein the step of depositing a metallic germanium layer includes depositing the metallic germanium layer having a thickness between approximately 40 nm and approximately 500 nm in a chemical vapor deposition process.

Claim 13. (Unchanged) The method as claimed in claim 9, wherein the step of patterning metallic germanium layer further includes the steps of:

depositing a photo resist layer over the metallic germanium layer;

exposing and developing the photo resist layer to form a photolithography image; and

etching the metallic germanium layer through the photolithography image.

Claim 14. (Unchanged) The method as claimed in claim 9, wherein the step of forming a dielectric stack further includes the steps of:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm on the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm on the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3000 nm on the nitride layer.

Claim 15. (Twice Amended) A method for etching a semiconductor wafer, the semiconductor wafer having a dielectric stack over a major surface thereof, the method comprising the steps of:

forming a germanium hard mask as a top most layer over the dielectric stack;

etching the dielectric stack through the germanium hard mask to form a dielectric hard mask over the major surface of the semiconductor wafer; and

etching the semiconductor wafer through the dielectric hard mask.

Claim 16. (Unchanged) The method as claimed in claim 15, wherein the step of forming a germanium hard mask includes the steps of:

depositing a layer of metallic germanium having a thickness equal to or greater than approximately 40 nm over the dielectric stack;

patterning the layer of metallic germanium to form the germanium hard mask.

Claim 17. (Unchanged) The method as claimed in claim 16, wherein the step of patterning the layer of metallic germanium further includes the steps of:

depositing a photo resist layer over the layer of metallic germanium;

patterning the photo resist layer to form a photolithography mask; and

etching the layer of metallic germanium through the photolithography mask.

Claim 18. (Unchanged) The method as claimed in claim 16, further comprising the step of stripping away the germanium hard mask after etching the dielectric stack and before etching the semiconductor wafer.

Claim 19. (Unchanged) The method as claimed in claim 18, wherein the step of stripping away the germanium hard mask includes the steps of:

oxidizing the layer of metallic germanium to convert the layer of metallic germanium into a layer of germanium oxide; and

removing the layer of germanium oxide.

Claim 20. (Unchanged) The method as claimed in claim 19, wherein the step of removing the layer of germanium oxide includes rising the semiconductor wafer in water.

Claim 21. (Unchanged) The method as claimed in claim 1, wherein the step of patterning the layer of metallic germanium comprises:

depositing a layer of photo resist;

etching the metallic germanium layer through the layer of photo resist; and

removing the layer of photo resist prior to the step of selectively etching the dielectric layer through the germanium hard mask

Claim 22 (New) The method of claim 7, further comprising removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask.

Claim 23 (New) The method of claim 13, further comprising removing the photoresist layer prior to selectively etching the dielectric layer through the germanium hard mask

Claim 24. (New) A method for etching a semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

depositing a layer of germanium over the dielectric layer;

depositing a photoresist layer over the germanium layer;

patterning the layer of metallic germanium through the photoresist layer to form a germanium hard mask over the dielectric layer;

removing the photoresist layer from over the germanium hard mask;

patterning the dielectric layer through the germanium hard a mask after removing the photoresist layer from over the germanium hard mask to form a dielectric hard mask over the semiconductor substrate; and

selectively etching the semiconductor substrate through the dielectric hard mask.

Claim 25. (New) The method as claimed in claim 24, further comprising the step of stripping away the germanium hard mask after patterning the dielectric layer to form the dielectric hard mask.

Claim 26. (New) The method as claimed in claim 25, wherein stripping away the layer of germanium comprises:

oxidizing the layer of germanium to form a layer of germanium oxide therefrom; and

removing the layer of germanium oxide.

Claim 27. (New) The method as claimed in claim 26, wherein removing the layer of germanium oxide comprises rinsing the semiconductor substrate in water.

Claim 28. (New) The method as claimed in claim 24, wherein depositing a layer of germanium comprises depositing the layer of germanium having a thickness between approximately 40 nm and approximately 500 nm.

Claim 29. (New) The method as claimed in claim 24, wherein patterning the layer of germanium further comprises:

exposing and developing the photoresist layer to form a photolithography image; and

etching the layer of metallic germanium through the photolithography image.

Claim 30. (New) The method as claimed in claim 24, further comprising forming a dielectric layer by:

forming a pad oxide layer having a thickness between approximately 5 nm and approximately 30 nm over the major surface of the semiconductor substrate;

depositing a nitride layer having a thickness between 50 nm and approximately 300 nm over the pad oxide layer; and

depositing a mask oxide layer having a thickness between 800 nm and approximately 3,000 nm over the nitride layer.

Claim 31. (New) A method for etching a semiconductor substrate having a dielectric layer over a major surface thereof, the method comprising the steps of:

depositing a layer of germanium over the dielectric layer;

patterning the layer of germanium to form a germanium hard mask;

patterning the dielectric layer through the germanium hard mask using a process selective to germanium to form an opening in the dielectric layer; and

selectively etching the semiconductor substrate through the opening in the dielectric layer.

Claim 32. (New) The method as claimed in claim 31, further comprising the step of stripping away the germanium hard mask after patterning the dielectric layer.